NMUX1237

2-channel analog multiplexer/demultiplexer

Rev. 1 — 12 July 2024 Product data sheet

1. General description

The NMUX1237 is a single-pole double-throw analog switch with a digital select input (S), two independent inputs/outputs (Y0 and Y1) and a common input/output (Z). The digital select input (S) supports 1.8 V logic thresholds independent of operating voltage. This feature enables compatibility in applications that combine low voltage digital I/Os with monitoring of mid voltage analog signals. The NMUX1237 is specifically designed for applications that are sensitive to signal overshoot.

2. Features and benefits

- Integrated suppression circuit to minimize signal overshoot
- 1.8 V control logic thresholds across supply operating range
- I_{off} circuitry
  - Enables wider latitude for power sequencing considerations
  - Isolates backflow between supply rail and any biased digital/analog input when V_{CC} = 0 V
  - Prevents any biased digital/analog input from backpowering V_{CC} when V_{CC} = 0 V
  - Analog switch path maintains isolation state
- Wide supply voltage range from 1.08 V to 5.5 V
- Very low ON resistance: 4 Ω
- Low supply current: 5 nA
- Rail-to-rail operation
- Bidirectional signal path
- Break-before-make switching
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C2b exceeds 750 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NMUX1237GW	-40 °C to +125 °C	TSSOP6	plastic thin shrink small outline package; 6 leads; body width 1.25 mm	SOT363-2

4. Marking

Table 2. Marking

Type number	Marking code[1]
NMUX1237	M1

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

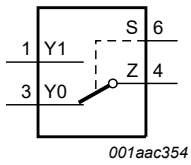


Fig. 1. Logic symbol

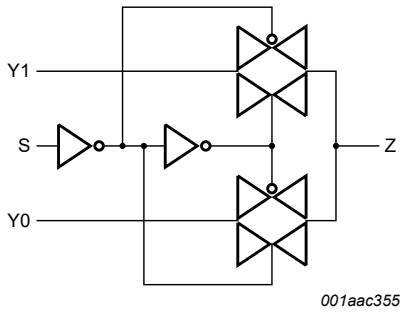
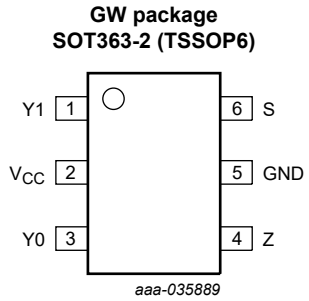


Fig. 2. Logic diagram

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
Y1	1	independent input or output
V_{CC}	2	supply voltage
Y0	3	independent input or output
Z	4	common input or output
GND	5	ground (0 V)
S	6	select input; must not be left floating

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7. Functional description

7.1. Overview

The NMUX1237 is an analog switch with a single pole that can be configured to select between one of two possible connection paths (SPDT). Each analog connection path is bi-directional, with similar electrical characteristics independent of the direction of signal propagation.

7.2. Key features

7.2.1. Overshoot suppression

Traditional analog switches will demonstrate output overshoot when switching between different channel inputs. This can be a concern in applications that are sensitive to signal integrity and precision performance. The NMUX1237 has a multi-stage design to reduce overshoot due to charge injection of the switch itself as well as output channel characteristics such as capacitive load and board parasitics, particularly parasitic inductance.

7.2.2. 1.8 V compatible digital logic thresholds

It is common for modern systems to operate digital signals from lower voltage nodes such as 1.8 V, while operating their analog signals at higher voltage nodes such as 3.3 V or 5.0 V. To remove the requirements for a voltage translation device, the NMUX1237 digital control pin maintains 1.8 V logic compatible thresholds at higher operating voltages, up to 5.5 V.

7.2.3. I_{off} protection circuitry of digital inputs

The NMUX1237 implements I_{off} protection circuitry on the digital control pins, isolating those pins from the internal circuits when the supply is unpowered (i.e., V_{CC} = 0 V). The ESD protection diodes on the digital input pins do not have a connection path to V_{CC}. If the digital input pins are biased when the V_{CC} pin is unpowered:

1. The high impedance of the digital inputs pins minimizes input current leakage.
2. The isolation between the digital input pins and the V_{CC} pin ensures no back-powering to the supply rail.

7.2.4. I_{off} protection circuitry of bi-directional analog inputs/outputs

The NMUX1237 implements I_{off} protection circuitry on the analog switch pins, isolating those pins from the internal circuits when the supply is unpowered (i.e., V_{CC} = 0 V). The ESD protection diodes on the analog switch pins do not have a connection path to V_{CC}. If the analog switch pins are biased when the V_{CC} pin is unpowered:

1. The high impedance of the analog pins minimizes input current leakage.
2. The isolation between the analog pins and the V_{CC} pin ensures no back-powering to the supply rail.
3. The high impedance of the analog switch path itself minimizes signal coupling across the switch.

Note: If the V_{CC} pin is powered up or down while there is an analog bias of pins Y0 or Y1, there will be a current draw into the respective Yx pin, and system design must ensure that the current draw is within the NMUX1237 recommended operating conditions.

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Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input S	Channel on
L	Y0
H	Y1

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	pin: V_{CC}	-0.5	+7.0	V
V_I	input voltage	pin S [1]	-0.5	+7.0	V
I_{IK}	input clamping current	V_I < -0.5 V or V_I > V_{CC} + 0.5 V pin S	-30	+30	mA
I_{SK}	switch clamping current	V_I < -0.5 V or V_I > V_{CC} + 0.5 V pins Yn, Z	-50	+50	mA
V_{SW}	switch voltage	enable and disable mode [2] pins Yn, Z	-0.5	V_{CC} + 0.5	V
I_{SW}	switch current	V_{SW} > -0.5 V or V_{SW} < V_{CC} + 0.5 V pins Yn, Z	-50	+50	mA
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	+150	°C

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.
[2] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.08	-	5.5	V
V_I	input voltage	pin S	0	-	5.5	V
V_{SW}	switch voltage	enable and disable mode [1]	0	-	V_{CC}	V
		V_{CC} = 0 V	0	-	5.5	V
I_{SW}	switch current		-50		+50	mA
T_{amb}	ambient temperature		-40	-	+125	°C

[1] To avoid sinking GND current from terminal Z when switch current flows in terminal Yn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no GND current will flow from terminal Yn. In this case, there is no limit for the voltage drop across the switch.

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10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	25 °C	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Typ [1]	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	pin S						
		V_{CC} = 5 V ± 10%	-	-	-	1.41	-	V
		V_{CC} = 3.3 V ± 10%	-	-	-	1.23	-	V
		V_{CC} = 1.8 V ± 10%	-	-	-	1.00	-	V
		V_{CC} = 1.2 V ± 10%	-	-	-	0.81	-	V
V_{IL}	LOW-level input voltage	pin S						
		V_{CC} = 5 V ± 10%	-	-	-	-	0.78	V
		V_{CC} = 3.3 V ± 10%	-	-	-	-	0.65	V
		V_{CC} = 1.8 V ± 10%	-	-	-	-	0.53	V
		V_{CC} = 1.2 V ± 10%	-	-	-	-	0.36	V
I_I	input leakage current	pin S; V_I = 5.5 V or GND						
		V_{CC} = 5 V ± 10%	±0.005	-	-	-1	1	µA
		V_{CC} = 3.3 V ± 10%	±0.005	-	-	-1	1	µA
		V_{CC} = 1.8 V ± 10%	±0.005	-	-	-1	1	µA
		V_{CC} = 1.2 V ± 10%	±0.005	-	-	-1	1	µA
$I_{P(OFF)}$	powered off leakage current	supply off, see Fig. 3						
		V_{CC} = 0 V; V_O = 0 V to 3.6 V, V_I = 0 V; V_O = 0, V_I = 0 V to 3.6 V	±0.01	-1	1	-5	5	µA
		V_{CC} = 0 V; V_O = 0 V to 5.5 V, V_I = 0 V; V_O = 0, V_I = 0 V to 5.5 V	±0.01	-4	4	-16	16	µA
$I_{S(OFF)}$	source off leakage current	switch off; see Fig. 3						
		V_{CC} = 5 V + 10%; V_O = 4.5 V and V_I = 1.5 V; V_O = 1.5 V and V_I = 4.5 V	±2	-55	55	-491	491	nA
		V_{CC} = 3.3 V + 10%; V_O = 3 V and V_I = 1 V; V_O = 1 V and V_I = 3 V	±2	-31	31	-248	248	nA
		V_{CC} = 1.8 V + 10%; V_O = 1.8 V and V_I = 1 V; V_O = 1 V and V_I = 1.8 V	±2	-64	64	-169	169	nA
		V_{CC} = 1.2 V + 10%; V_O = 1.2 V and V_I = 1 V; V_O = 1 V and V_I = 1.2 V	±2	-33	33	-139	139	nA

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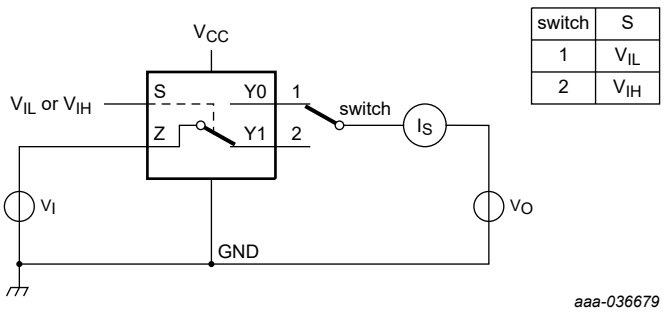
Symbol	Parameter	Conditions	25 °C	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Typ [1]	Min	Max	Min	Max	
$I_{S(ON)}$	channel on leakage current	switch on; see Fig. 4						
		V_{CC} = 5 V + 10%; V_O = V_I = 4.5 V or 1 V	±2	-157	157	-1088	1088	nA
		V_{CC} = 3.3 V + 10%; V_O = V_I = 3 V or 1 V	±2	-103	103	-547	547	nA
		V_{CC} = 1.8 V + 10%; V_O = V_I = 1.62 V or 1 V	±2	-75	75	-331	331	nA
		V_{CC} = 1.2 V + 10%; V_O = V_I = 1 V or 0.8 V	±2	-52	52	-260	260	nA
$I_{D(ON)}$	channel on leakage current	switch on; see Fig. 4						
		V_{CC} = 5 V + 10%; V_O = V_I = 4.5 V or 1 V	±2	-157	157	-1088	1088	nA
		V_{CC} = 3.3 V + 10%; V_O = V_I = 3 V or 1 V	±2	-103	103	-547	547	nA
		V_{CC} = 1.8 V + 10%; V_O = V_I = 1.62 V or 1 V	±2	-75	75	-331	331	nA
		V_{CC} = 1.2 V + 10%; V_O = V_I = 1 V or 0.8 V	±2	-52	52	-260	260	nA
I_{CC}	supply current	pin S; V_I = 5.5 V or GND						
		V_{CC} = 5 V + 10%	0.005	-	-	-	1.9	µA
		V_{CC} = 3.3 V + 10%	0.003	-	-	-	0.7	µA
		V_{CC} = 1.8 V + 10%	0.002	-	-	-	0.3	µA
		V_{CC} = 1.2 V + 10%	0.001	-	-	-	0.3	µA

[1] Typical values are measured at T_{amb} = 25 °C, V_{CC} = 5.0 V, 3.3 V, 1.8 V, and 1.2 V

10.1. Test circuits



switch	S
1	V_{IL}
2	V_{IH}

Fig. 3. Test circuit for measuring OFF-state leakage current

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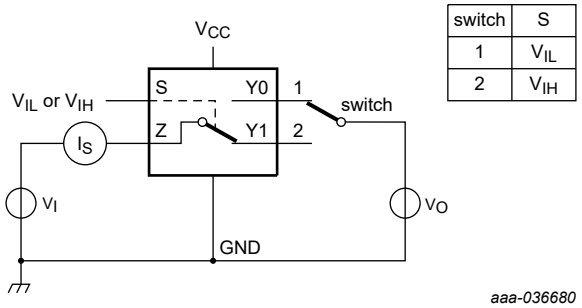

switch	S
1	V_{IL}
2	V_{IH}

Fig. 4. Test circuit for measuring ON-state leakage current

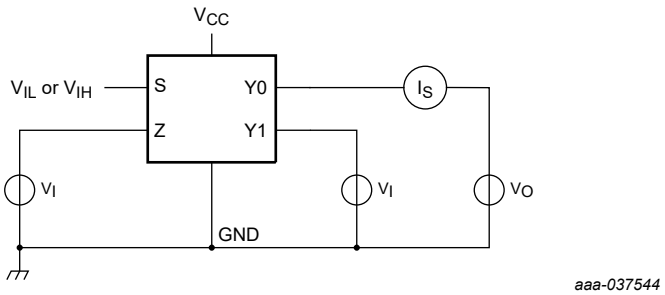

Fig. 5. Test circuit for measuring powered OFF-state leakage current

10.2. ON resistance

Table 8. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground 0 V); for test circuit see Fig. 6.

Symbol	Parameter	Conditions	25 °C	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Typ [1]	Min	Max	Min	Max	
$R_{ON(peak)}$	ON resistance (peak)	V_I = GND to V_{CC}; I_{SW} = 10 mA; see Fig. 6						
		V_{CC} = 5 V ± 10%	4	-	9	-	9	Ω
		V_{CC} = 3.3 V ± 10%	7	-	13	-	14	Ω
		V_{CC} = 1.8 V ± 10%	32	-	68	-	68	Ω
		V_{CC} = 1.2 V ± 10%	68	-	100	-	100	Ω
ΔR_{ON}	ON resistance matching	V_I = GND to V_{CC}; I_{SW} = 10 mA; see Fig. 6						
		V_{CC} = 5 V ± 10%	0.11	-	1	-	1	Ω
		V_{CC} = 3.3 V ± 10%	0.11	-	1	-	1	Ω
		V_{CC} = 1.8 V ± 10%	0.12	-	6	-	6	Ω
		V_{CC} = 1.2 V ± 10%	0.21	-	17	-	17	Ω
$R_{ON(flat)}$	ON resistance (flatness)	V_I = GND to V_{CC}; I_{SW} = 10 mA [2]						
		V_{CC} = 5 V ± 10%	1	-	3	-	3	Ω
		V_{CC} = 3.3 V ± 10%	3	-	7	-	7	Ω
		V_{CC} = 1.8 V ± 10%	26	-	62	-	62	Ω
		V_{CC} = 1.2 V ± 10%	58	-	88	-	88	Ω

[1] Typical values are measured at T_{amb} = 25 °C, V_{CC} = 5.0 V, 3.3 V, 1.8 V, 1.2 V
[2] Flatness is defined as the difference between the maximum and minimum value of ON resistance measured at identical V_{CC} and temperature.

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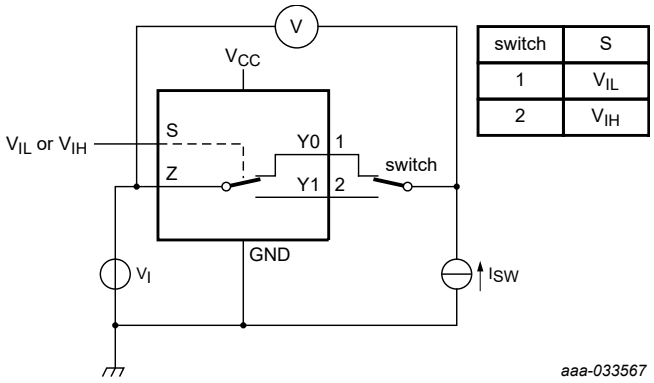
10.3. ON resistance test circuit



switch	S
1	V_{IL}
2	V_{IH}

$R_{ON} = V_{SW} / I_{SW}$

Fig. 6. Test circuit for measuring ON resistance

11. Dynamic characteristics

Table 9. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuits see Fig. 7 through Fig. 12.

Symbol	Parameter	Conditions	25 °C	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Typ [1]	Min	Max	Min	Max	
t_t	transition time between channels	S to Z R_L = 200 Ω; C_L = 15 pF						
		V_{CC} = 5 V ± 10%; V_I = 3 V	23	-	34	-	35	ns
		V_{CC} = 3.3 V ± 10%; V_I = 2 V	43	-	63	-	65	ns
		V_{CC} = 1.8 V ± 10%; V_I = 1 V	57	-	103	-	106	ns
		V_{CC} = 1.2 V ± 10%; V_I = 1 V	163	-	505	-	505	ns
t_{b-m}	break-before-make time	R_L = 200 Ω; C_L = 15 pF						
		V_{CC} = 5 V ± 10%; V_I = 3 V	211	10	-	10	-	ns
		V_{CC} = 3.3 V ± 10%; V_I = 2 V	283	10	-	10	-	ns
		V_{CC} = 1.8 V ± 10%; V_I = 1 V	321	10	-	10	-	ns
		V_{CC} = 1.2 V ± 10%; V_I = 1 V	1872	10	-	10	-	ns
Q_{inj}	charge injection	R_{gen} = 0 Ω; C_L = 1 nF						
		V_{CC} = 5 V ± 10%; V_{gen} = 0.5 × V_{CC}	5	-	-	-	-	pC
		V_{CC} = 3.3 V ± 10%; V_{gen} = 0.5 × V_{CC}	4	-	-	-	-	pC
		V_{CC} = 1.8 V ± 10%; V_{gen} = 0.5 × V_{CC}	2	-	-	-	-	pC
		V_{CC} = 1.2 V ± 10%; V_{gen} = 0.5 × V_{CC}	2	-	-	-	-	pC

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Symbol	Parameter	Conditions	25 °C	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Typ [1]	Min	Max	Min	Max	
α_{ISO}	isolation (OFF-state)	R_L = 50 Ω; C_L = 5 pF; f = 1 MHz						
		V_{CC} = 5 V ± 10%	-82	-	-	-	-	dB
		V_{CC} = 3.3 V ± 10%	-82	-	-	-	-	dB
		V_{CC} = 1.8 V ± 10%	-82	-	-	-	-	dB
		V_{CC} = 1.2 V ± 10%	-82	-	-	-	-	dB
		R_L = 50 Ω; C_L = 5 pF; f = 10 MHz						
		V_{CC} = 5 V ± 10%	-62	-	-	-	-	dB
		V_{CC} = 3.3 V ± 10%	-62	-	-	-	-	dB
		V_{CC} = 1.8 V ± 10%	-61	-	-	-	-	dB
		V_{CC} = 1.2 V ± 10%	-61	-	-	-	-	dB
Xtalk	crosstalk	R_L = 50 Ω; C_L = 5 pF; f = 1 MHz						
		V_{CC} = 5 V ± 10%	-77	-	-	-	-	dB
		V_{CC} = 3.3 V ± 10%	-77	-	-	-	-	dB
		V_{CC} = 1.8 V ± 10%	-78	-	-	-	-	dB
		V_{CC} = 1.2 V ± 10%	-82	-	-	-	-	dB
		R_L = 50 Ω; C_L = 5 pF; f = 10 MHz						
		V_{CC} = 5 V ± 10%	-57	-	-	-	-	dB
		V_{CC} = 3.3 V ± 10%	-57	-	-	-	-	dB
		V_{CC} = 1.8 V ± 10%	-58	-	-	-	-	dB
		V_{CC} = 1.2 V ± 10%	-61	-	-	-	-	dB
BW	bandwidth	R_L = 50 Ω; C_L = 5 pF						
		V_{CC} = 5 V ± 10%	196	-	-	-	-	MHz
		V_{CC} = 3.3 V ± 10%	179	-	-	-	-	MHz
		V_{CC} = 1.8 V ± 10%	119	-	-	-	-	MHz
		V_{CC} = 1.2 V ± 10%	90	-	-	-	-	MHz
C_I	input capacitance	pin S	2	-	-	-	4	pF
$C_{S(OFF)}$	OFF-state capacitance	f = 1 MHz						
		V_{CC} = 5 V ± 10%	10	-	-	-	-	pF
		V_{CC} = 3.3 V ± 10%	11	-	-	-	-	pF
		V_{CC} = 1.8 V ± 10%	12	-	-	-	-	pF
		V_{CC} = 1.2 V ± 10%	12	-	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance	f = 1 MHz						
		V_{CC} = 5 V ± 10%	27	-	-	-	-	pF
		V_{CC} = 3.3 V ± 10%	30	-	-	-	-	pF
		V_{CC} = 1.8 V ± 10%	32	-	-	-	-	pF
		V_{CC} = 1.2 V ± 10%	27	-	-	-	-	pF
$C_{D(ON)}$	ON-state capacitance	f = 1 MHz						
		V_{CC} = 5 V ± 10%	27	-	-	-	-	pF
		V_{CC} = 3.3 V ± 10%	30	-	-	-	-	pF
		V_{CC} = 1.8 V ± 10%	32	-	-	-	-	pF
		V_{CC} = 1.2 V ± 10%	27	-	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C, V_{CC} = 5.0 V, 3.3 V, 1.8 V, and 1.2 V

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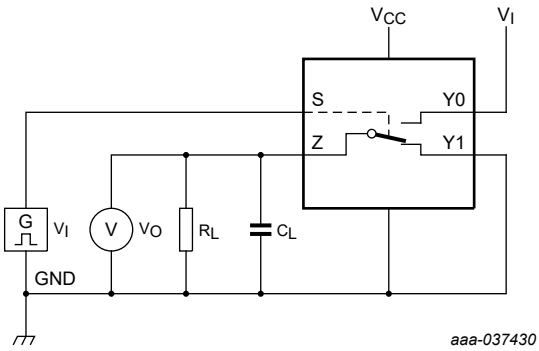
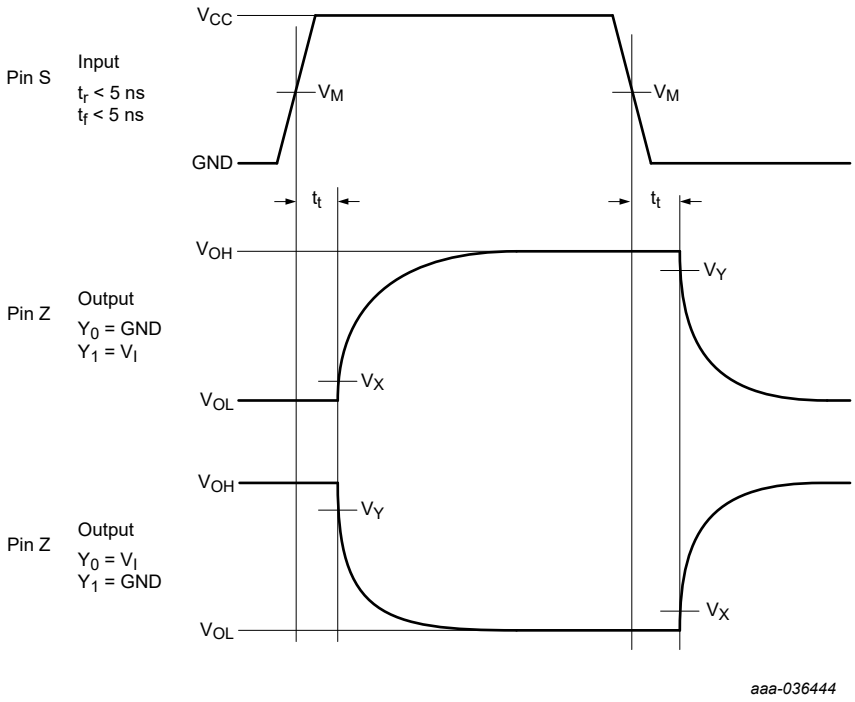
11.1. Waveforms and test circuits



a. Test circuit



b. Input and output measurement points.

Measurement points are given in Table 10.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 7. Test circuit for measuring transition time between channels

Table 10. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
1.08 V to 5.5 V	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 10%	V_{OH} - 10%

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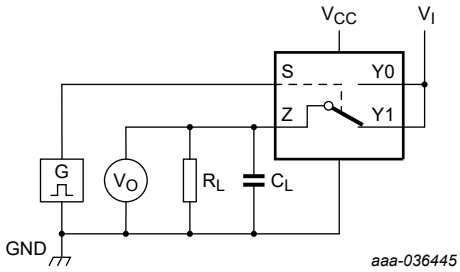
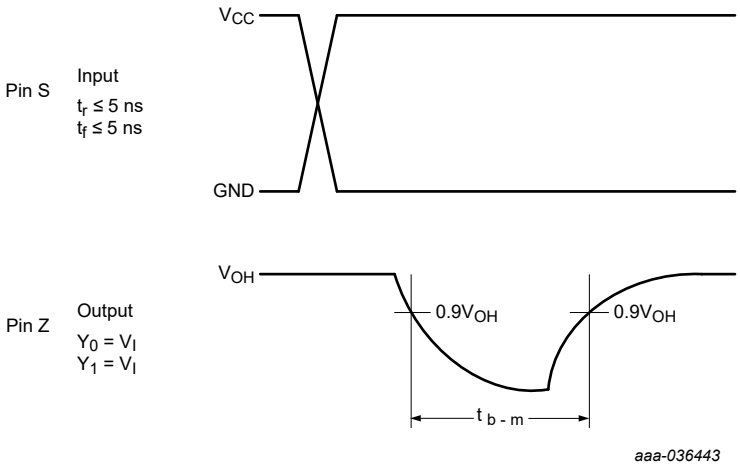


a. Test circuit

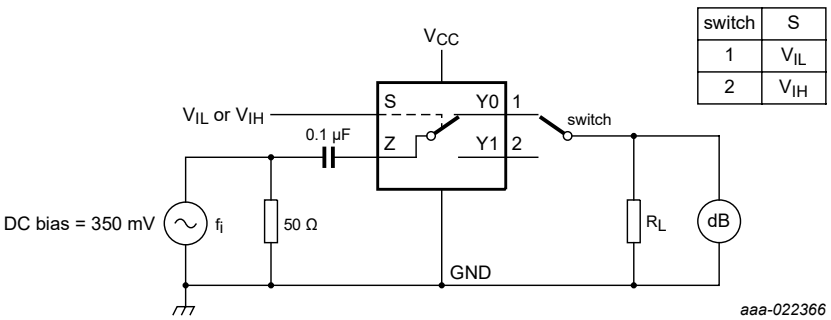


b. Input and output measurement points

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 8. Test circuit for measuring break-before-make timing

11.2. Test circuits



Adjust f_i voltage to obtain 0 dBm level at output. Increase f_i frequency until dB meter reads -3 dB.

Fig. 9. Test circuit for measuring the frequency response when switch is in ON-state

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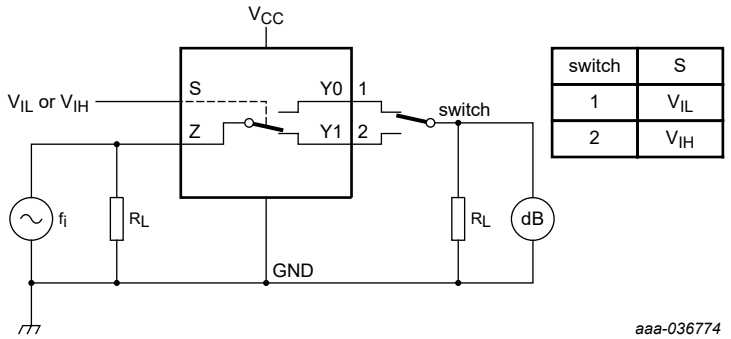
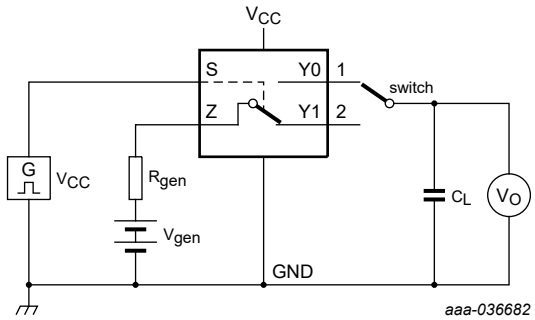


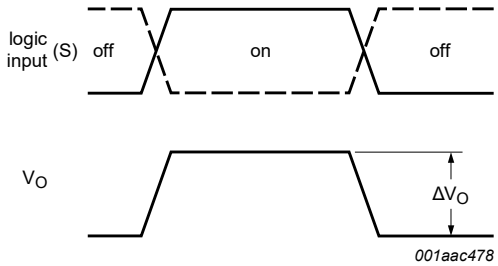
switch	S
1	V_{IL}
2	V_{IH}

Adjust f_i voltage to obtain 0 dBm level at input.

Fig. 10. Test circuit for measuring isolation (OFF-state)



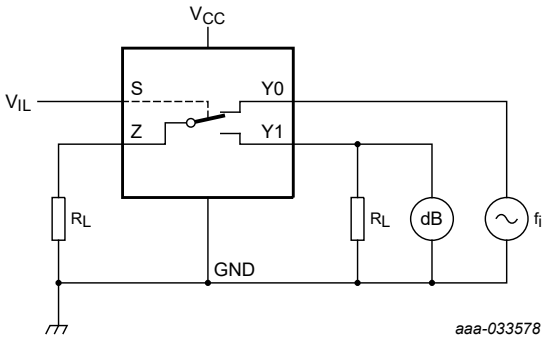
a. Test circuit



b. Input and output pulse definitions

$Q_{inj} = \Delta V_O \times C_L$;
ΔV_O = output voltage variation;
R_{gen} = generator resistance;
V_{gen} = generator voltage.

Fig. 11. Test circuit for measuring charge injection



f_i voltage source: Z_O = 50 Ω. The f_i voltage level is set for R_L = 50 Ω; DC = 0.5V_{CC}; AC = 0 dBm.

Fig. 12. Test circuit for measuring crosstalk between switches

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12. Applications

The NMUX1237 is a versatile CMOS bidirectional (SPDT) single-pole double-throw analog switch with digital control pins that support 1.8 V logic thresholds independent of the supply voltage. Supporting a wide supply voltage range of 1.08 V to 5.5 V, the device additionally features integrated circuitry to minimize analog signal overshoot when switching between channels. No power sequencing is required, as both digital and analog back-power protection are implemented.

12.1. Typical application schematic

A typical example is provided in Fig. 13. In this example, the NMUX1237 is used to control the input to the op-amp in the programmable low-side current sink application circuit. It allows for a fast disconnect when no current is required through the circuit's load. In this example, the power supplies for the analog switch and the op-amp circuit are activated before the rails of the DAC and MCU. As a result, the analog switch will by default connect the op-amp input to GND and prevent any current from flowing through the load before the DAC is properly initialized. Once the DAC is initialized, the NMUX1237 can then connect it to the op-amp input to programmatically change the current going through the load.

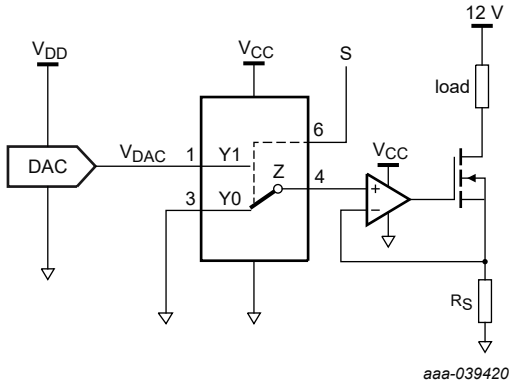

Fig. 13. Programmable low-side current sink circuit

Table 11. Design requirements

Condition	Value
I_{OUT} current range	0 to 200 mA
1.8 V control logic	
Supply voltage	5 V (1.08 V to 5.5 V supported)
Input analog signal range	0 V to V_{CC}
Ouput range of DAC (V_{ref})	4.096 V (DAC output 0V to 4.096 V)
Required overshoot	0 V (Ensures no predictable current across load)

Calculating R_S for maximum V_{DAC}/I_{OUT} value:

$$R_S = \frac{V_{DAC}}{I_{OUT}} = \frac{4.096\ V}{200\ mA} \approx 20.5\ \Omega\ (max) \quad (1)$$

A rough estimate of the maximum supported resistive load can be calculated as:

$$R_{LOAD(max)} = \frac{V_{CC} - R_S I_{OUT}}{I_{OUT}} = \frac{12\ V - (20.5\ \Omega)(0.2\ A)}{0.2\ A} = 39.5\ \Omega\ (max) \quad (2)$$

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To determine the true maximum load, the NMOS compliance voltage should either be measured or recorded from the datasheet.

$$R_{LOAD(max)} = \frac{V_{CC} - V_{Compliance(NMOS)} - R_S I_{OUT}}{I_{OUT}} \quad (3)$$

12.2. Overshoot suppression

Fig. 14 demonstrates the integrated suppression circuit that eliminates signal overshoot when changing between analog channels. In this example, the NMUX1237 is powered with a supply voltage of 5 V. The analog inputs Y0 and Y1 are biased with GND and 3.3 V, respectively. The S control pin switches the output between GND and 3.3 V, and output voltage is observed on pin Z.

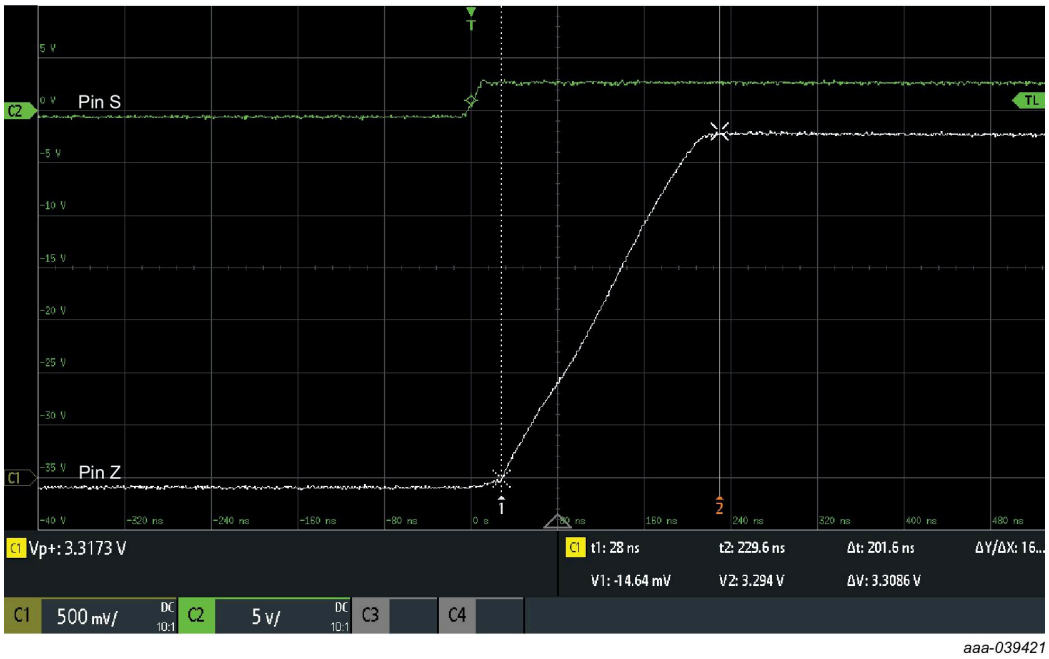

Fig. 14. NMUX1237 eliminates overshoot

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12.3. Example application circuits

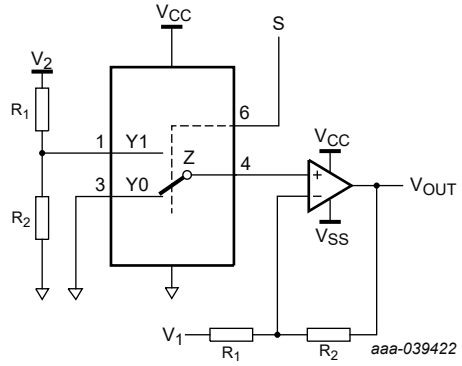
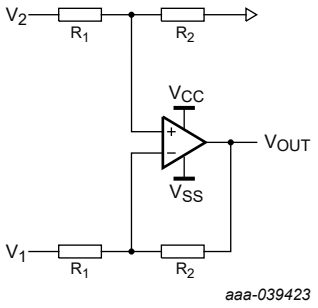
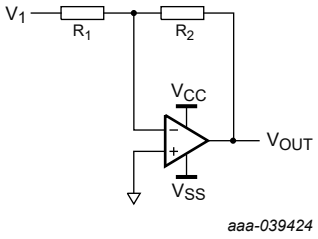


Fig. 15. Programmable op-amp circuit

In the example in Fig. 15, an NMUX1237 is used to create a selectable op-amp circuit that enables two different configurations. When the channel path Y0 is connected, the circuit will function as an inverting op-amp configuration, while connecting the Y1 path will result in a differential amplifier configuration. The resulting circuits are further explained in Fig. 16



$V_{out} = (R_2/R_1)(V_2 - V_1)$
Differential amplifier when channel Y1 selected



$V_{out} = -(R_2/R_1)(V_1)$
Inverting op-amp configuration when channel Y0 selected.

Fig. 16. Configurations for NMUX1237

The design can be further improved by substituting a DAC output for V_2. This would enable a programmable difference amplifier, with the resulting transfer function shown in Equation 4. The V_{DAC} voltage value woud provide an offset for the inverted waveform.

$$V_{OUT} = \frac{(V_{DAC} - V_1)\,R_2}{R_1} \quad (4)$$

where V_{DAC} is offset applied to inverted signal Equation 4.

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12.4. Layout example and recommendations

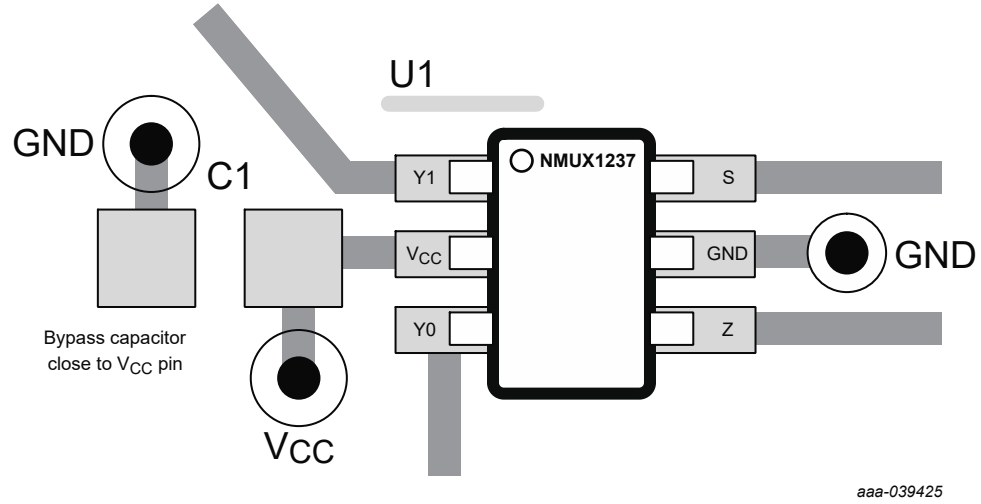

Fig. 17. Example layout with NMUX1237

As with all board designs, proper layout techniques should be employed. Some quick good layout practices and considerations are listed below for quick reference.

- Ceramic capacitors with low ESR should be used to properly decouple or bypass power-supply pins. Ceramic capacitors with high temperature coefficients and low dissipation factors include X5R, X7R and NP0. The recommended minimum value is 0.1 µF.
- For improved noise suppression, additional bypass capacitors can be implemented. It is a common practice to use two different capacitor values to ensure proper filtering of both low-frequency and high-frequency transients. The smaller capacitor, typically in a 0402 package, is placed very near the device pin, while the larger capacitor is positioned farther away.
- To minimize coupling and improve performance all switching nets should travel across a uniform ground plane. Reducing crosstalk can also be achieved by separating traces with a small polygon ground plane.
- Net traces should only have serpentine or 45° bend. Sharper bends, such as 90° should be avoided.

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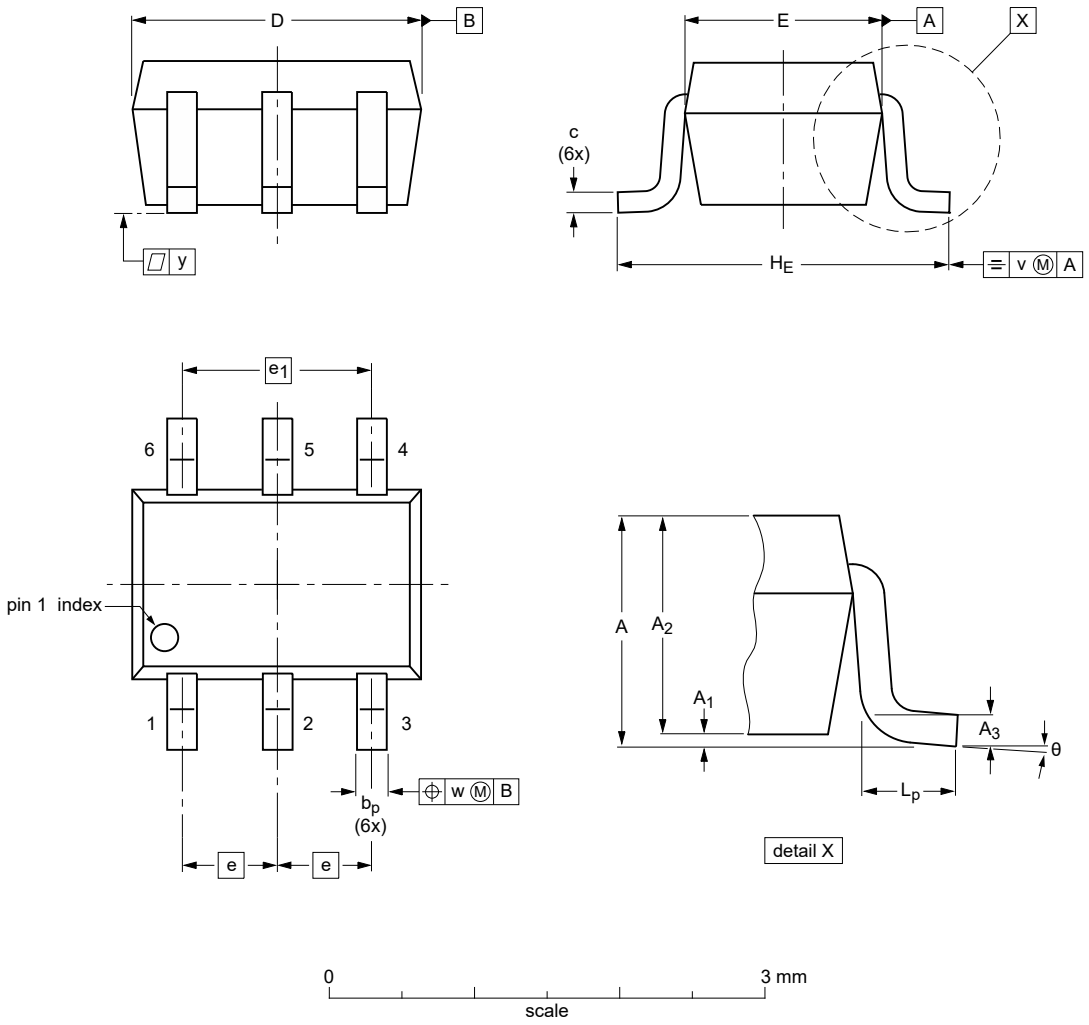
13. Package outline

TSSOP6: plastic thin shrink small outline package; 6 leads; body width 1.25 mm **SOT363-2**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	e_1	H_E	L_p	v	w	y	θ
mm	max	1.1	0.1	1.0	0.15	0.30	0.25	2.2	1.35	0.65	1.3	2.4	0.46	0.3	0.1	0.1	8°
	min	0.8	0	0.8		0.15	0.08	1.8	1.15			1.8	0.26				0°

Note
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

sot363-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT363-2		MO-203	SC-88A			~~21-12-15~~ 21-12-16

Fig. 18. Package outline SOT363-2 (TSSOP6)

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14. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

15. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NMUX1237 v.1	20240712	Product data sheet	-	-

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Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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